

Fig. 1A PRIOR ART

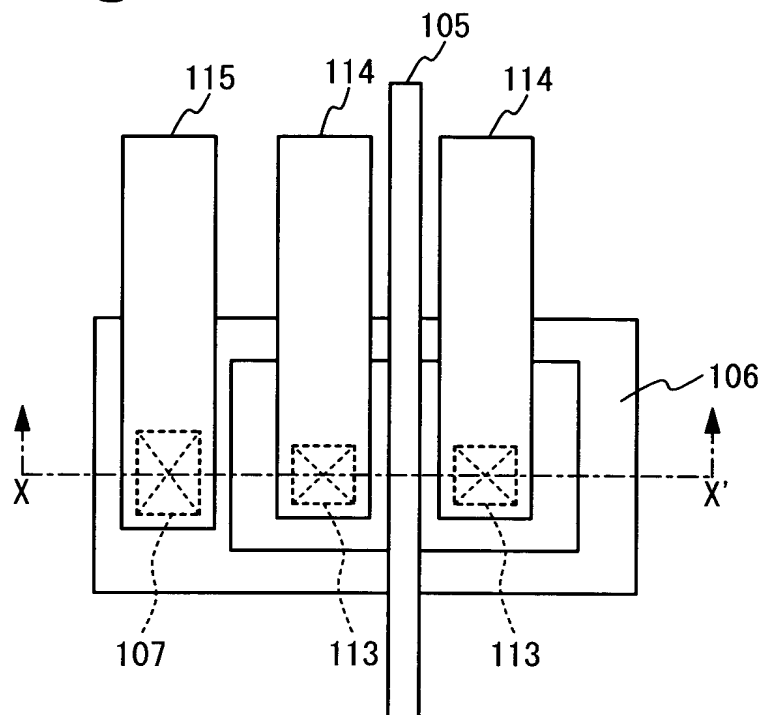


Fig. 1B PRIOR ART

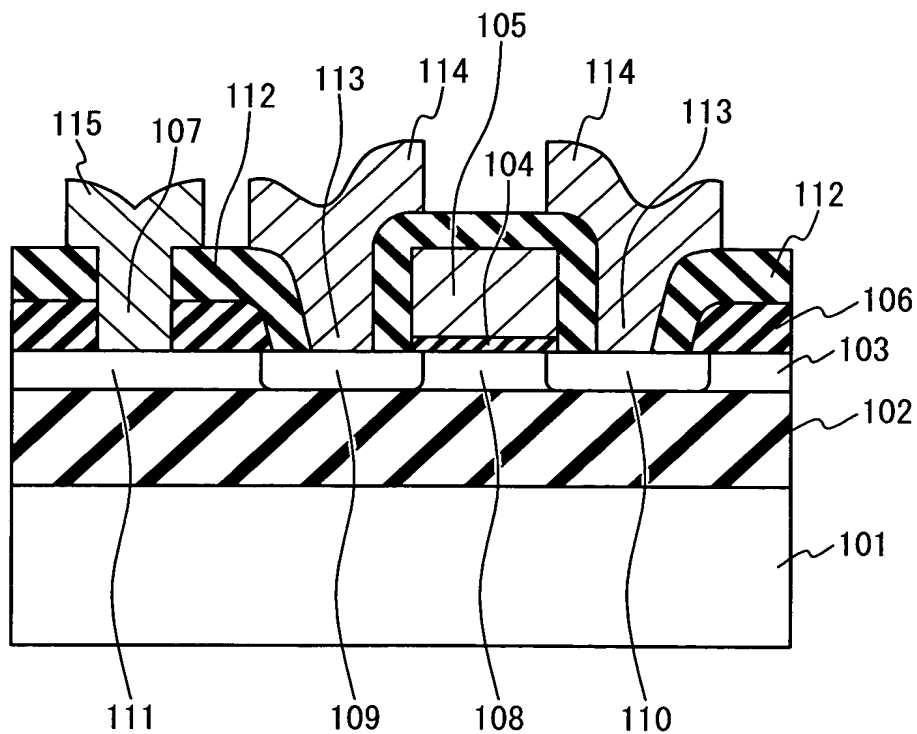


Fig. 2A PRIOR ART

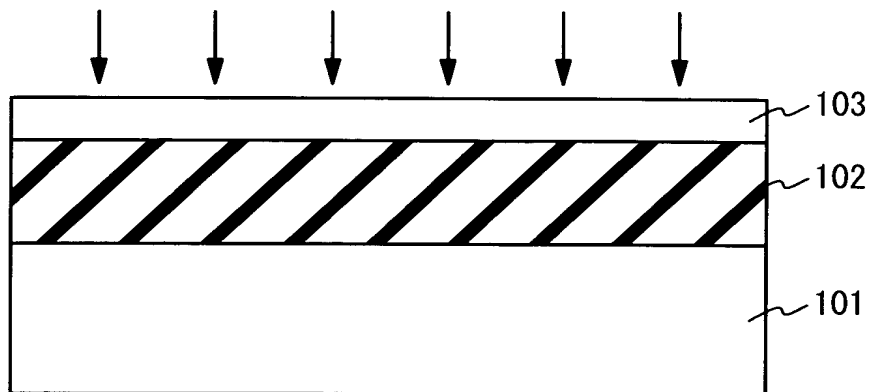


Fig. 2B PRIOR ART

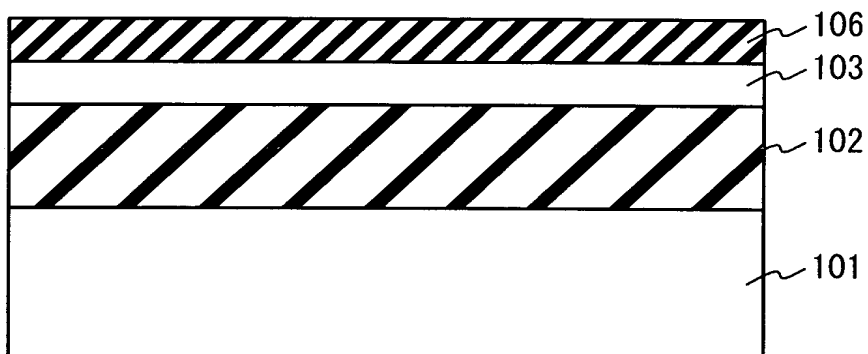


Fig. 2C PRIOR ART

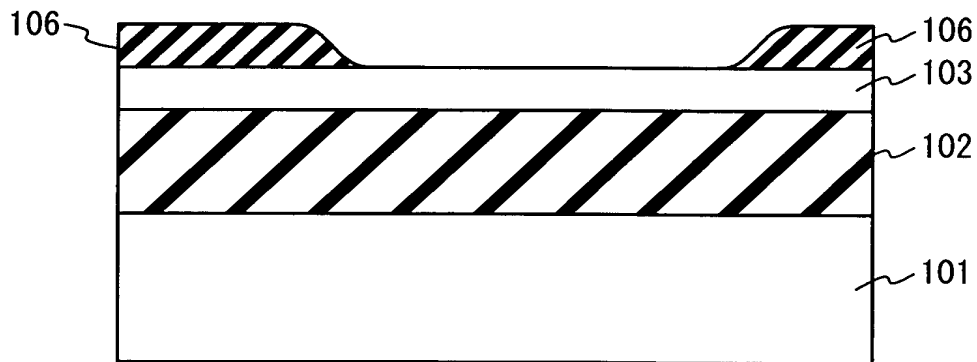


Fig. 3A PRIOR ART

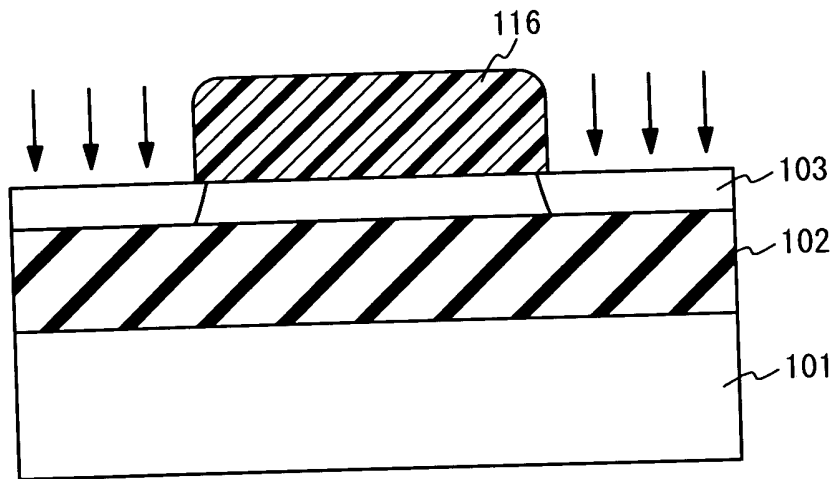


Fig. 3B PRIOR ART

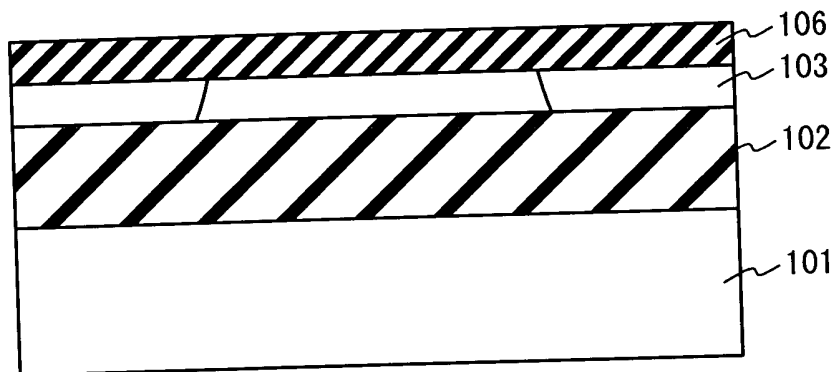


Fig. 3C PRIOR ART

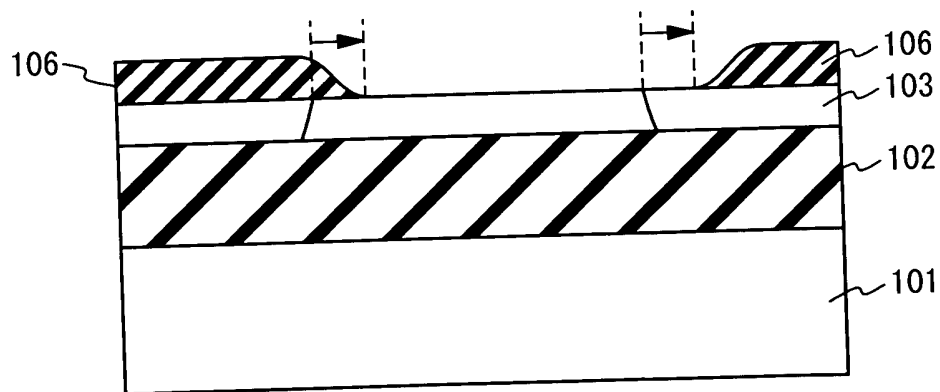


Fig. 4 PRIOR ART

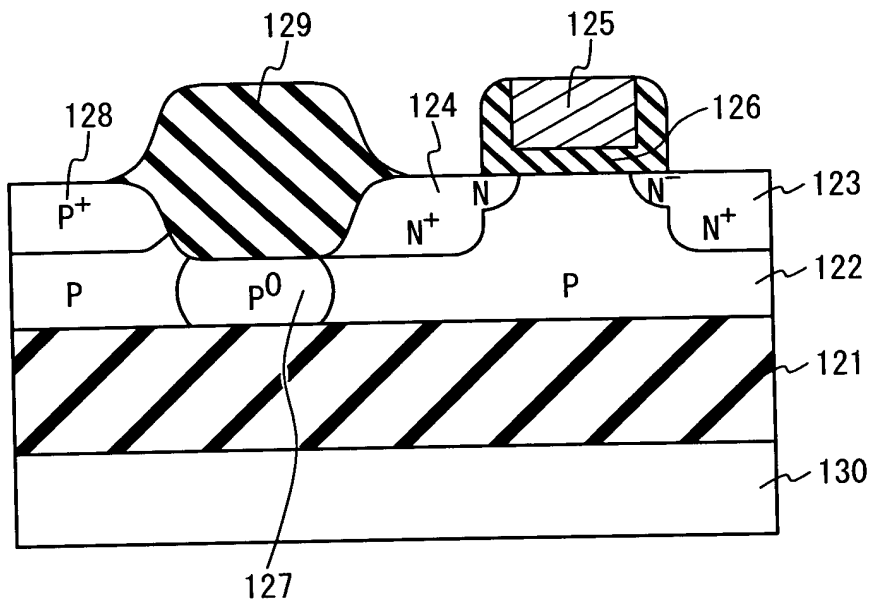


Fig. 5 PRIOR ART

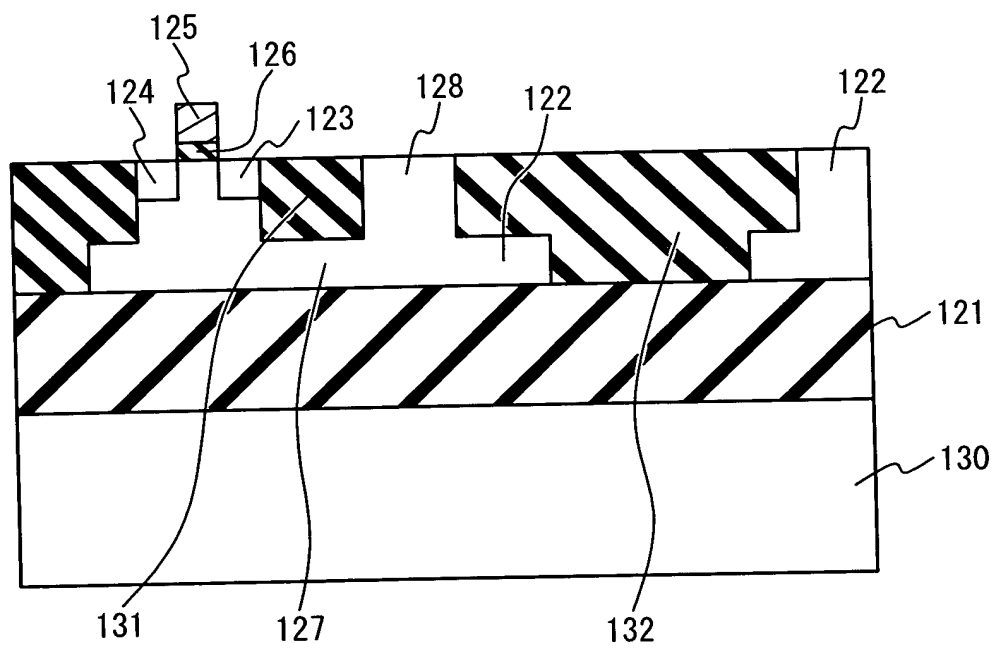
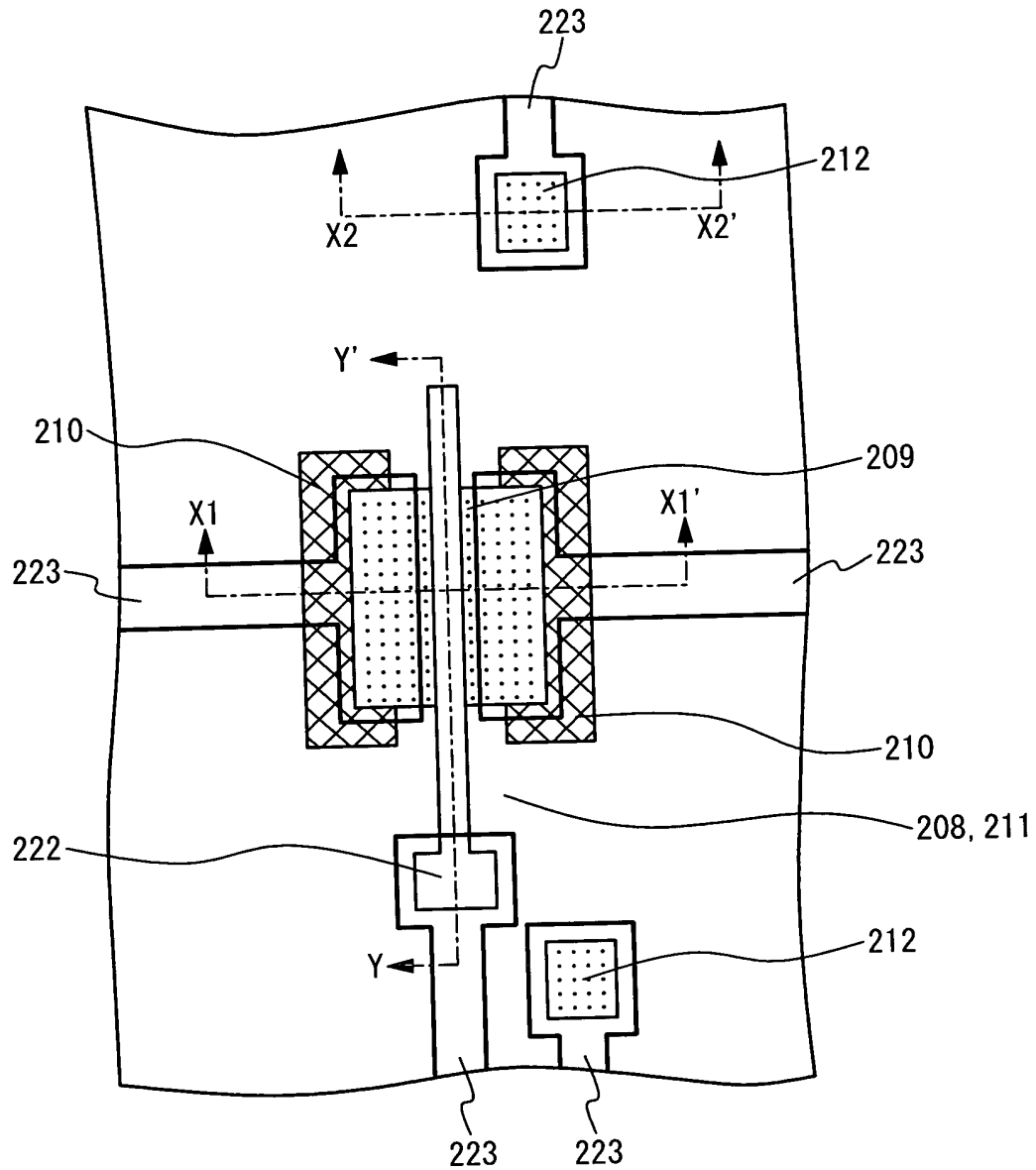
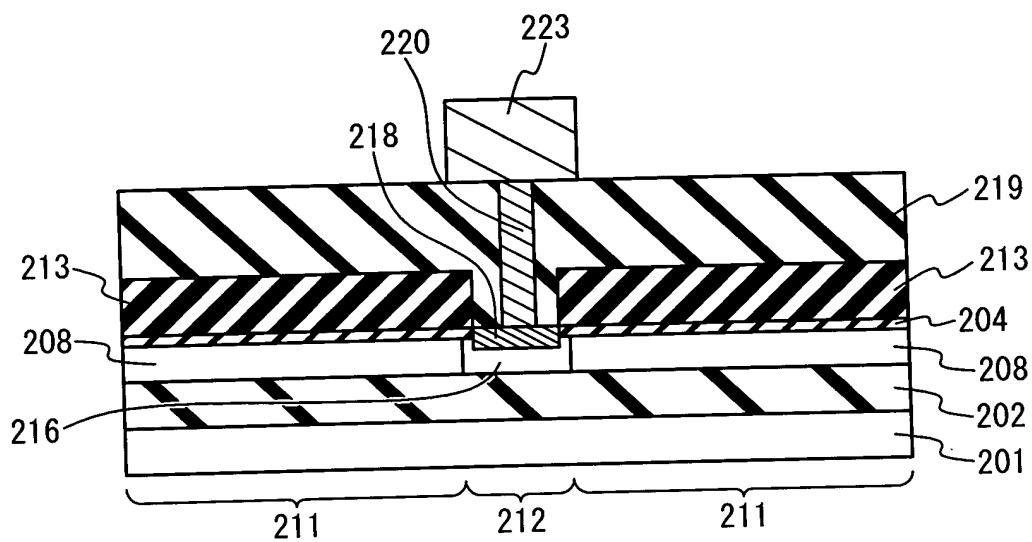


Fig. 6



This cross-sectional view shows a semiconductor device with a central gate structure. The device includes a substrate (201) with a thin layer (202) on top. A central gate stack (209) is formed on the substrate, consisting of a gate dielectric (214) and a gate electrode (218). The gate stack is flanked by side regions (210) and end regions (211). The side regions (210) contain a layer (204) and a layer (208). The end regions (211) contain a layer (204) and a layer (208). The device is covered by a top layer (223) and a bottom layer (203). Various other layers and structures are labeled with reference numerals 201 through 223.

Fig. 7C



F i g . 8

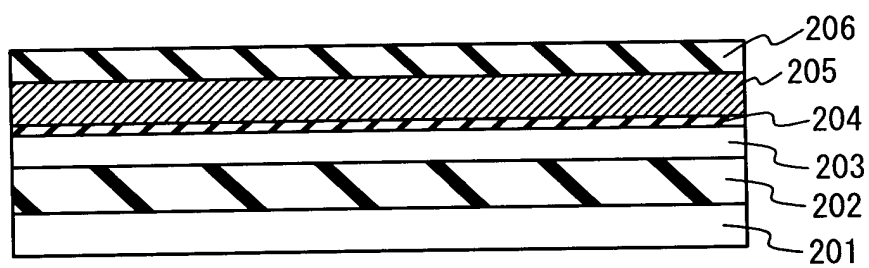


Fig. 9

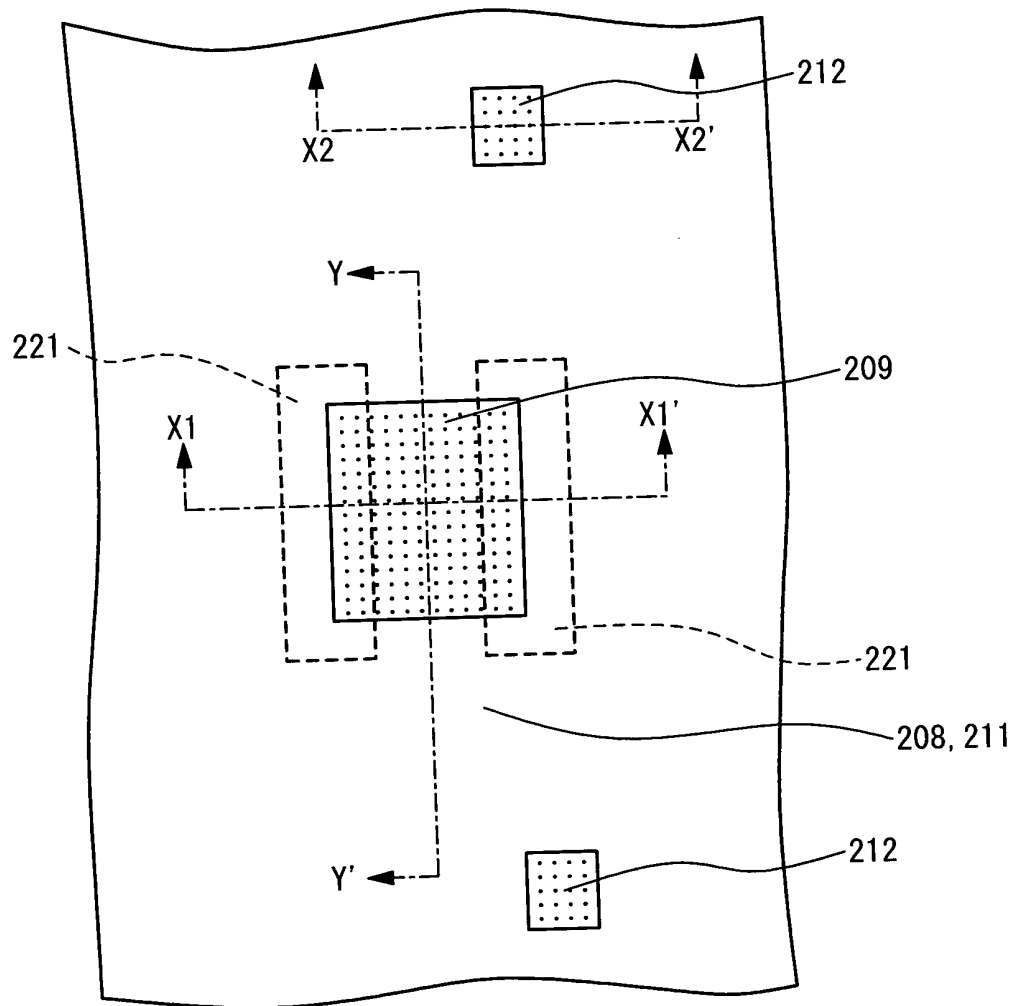


Fig. 10A

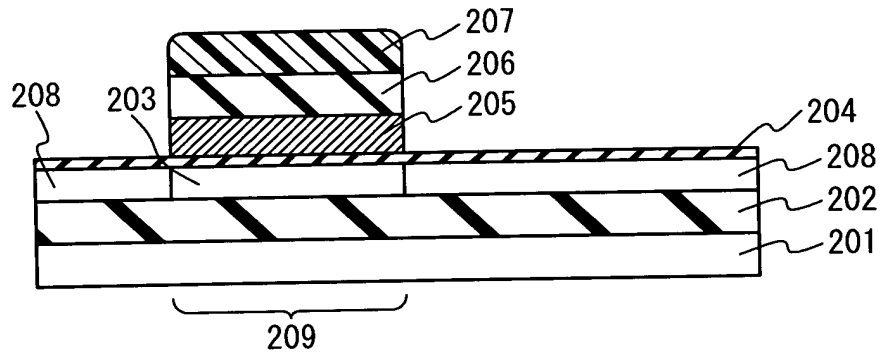


Fig. 10B

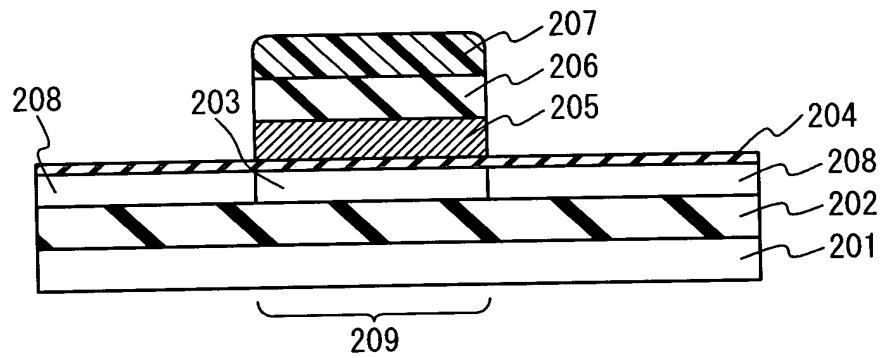


Fig. 10C

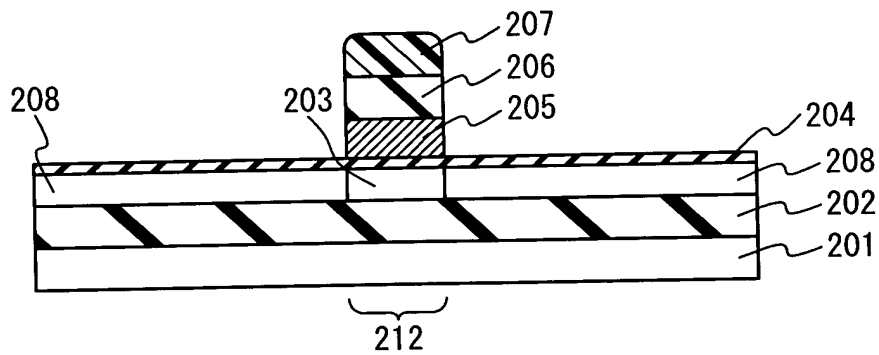


Fig. 11

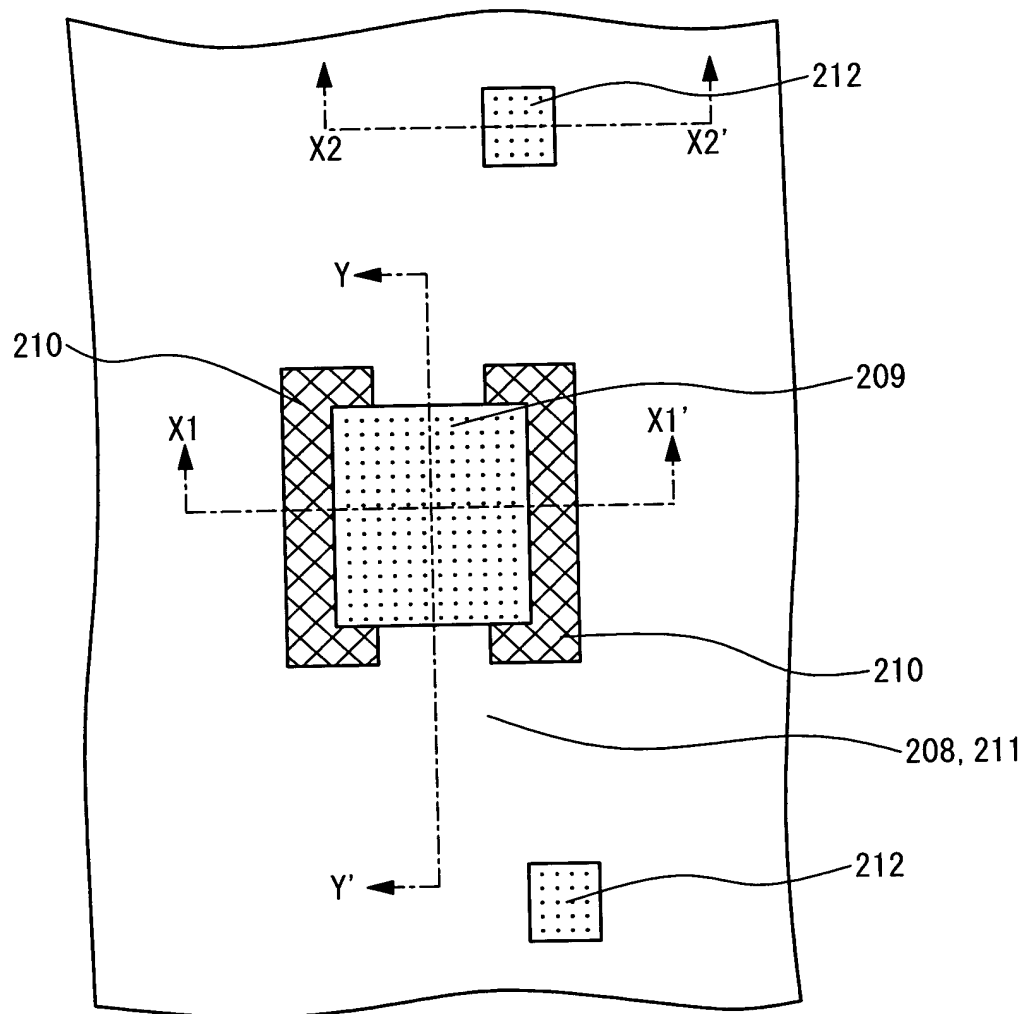


Fig. 12A

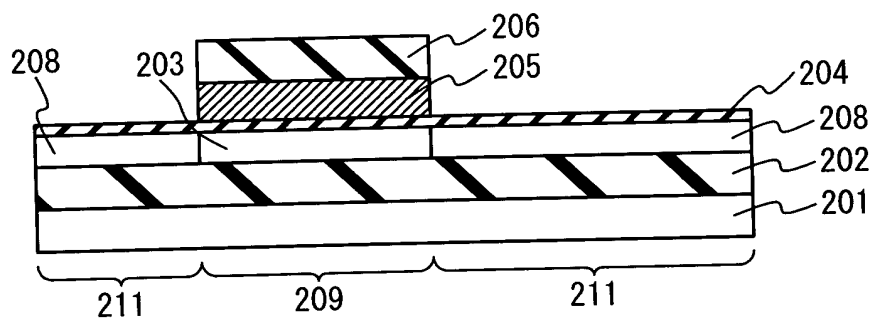


Fig. 12B

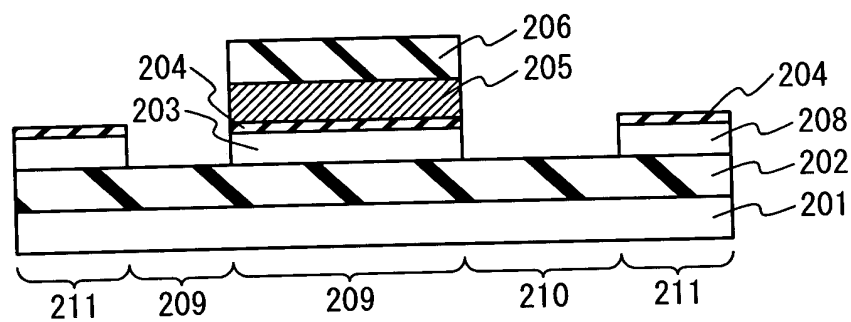


Fig. 12C

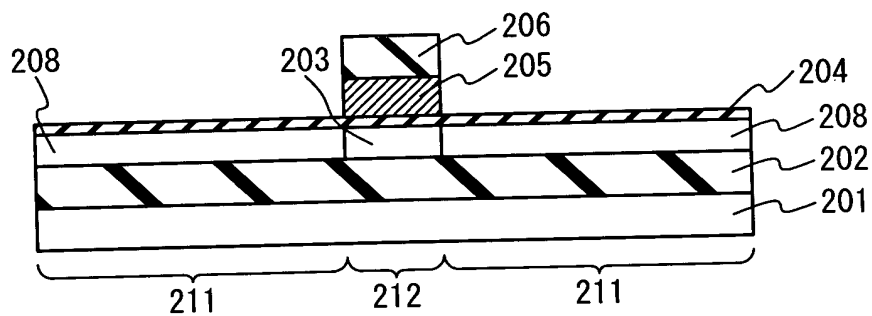


Fig. 13A

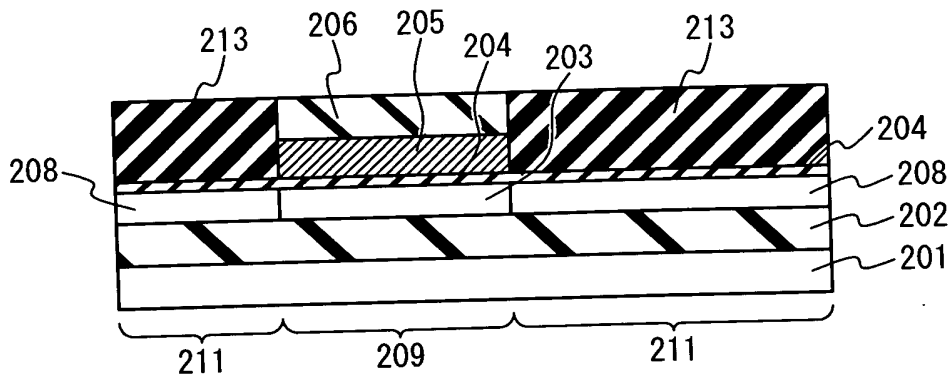


Fig. 13B

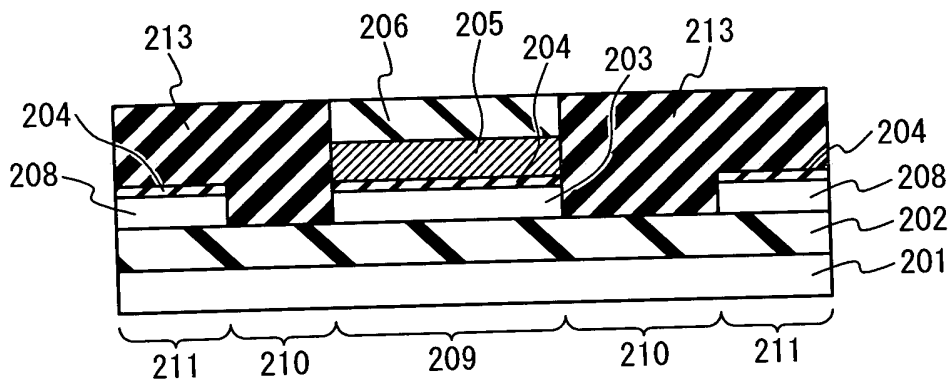


Fig. 13C

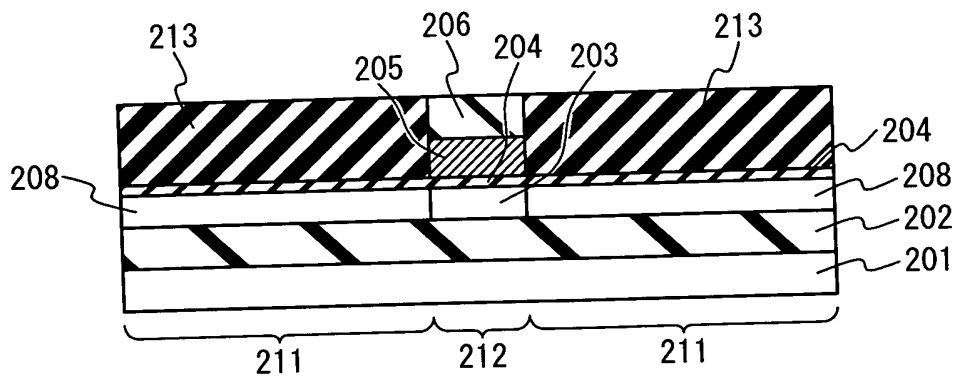


Fig. 14A

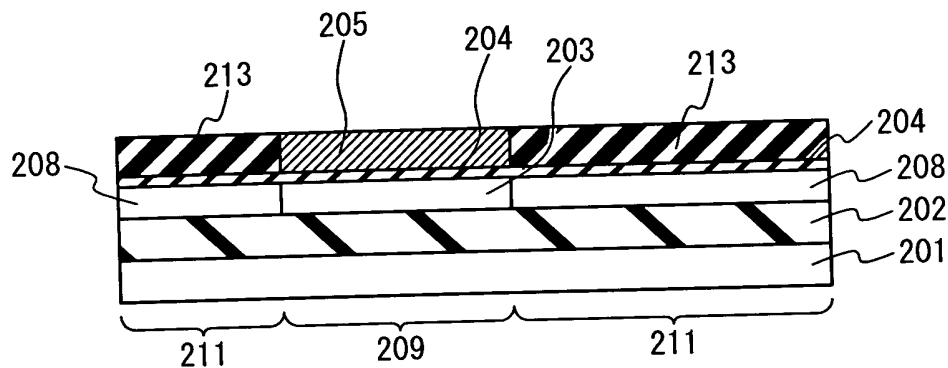


Fig. 14B

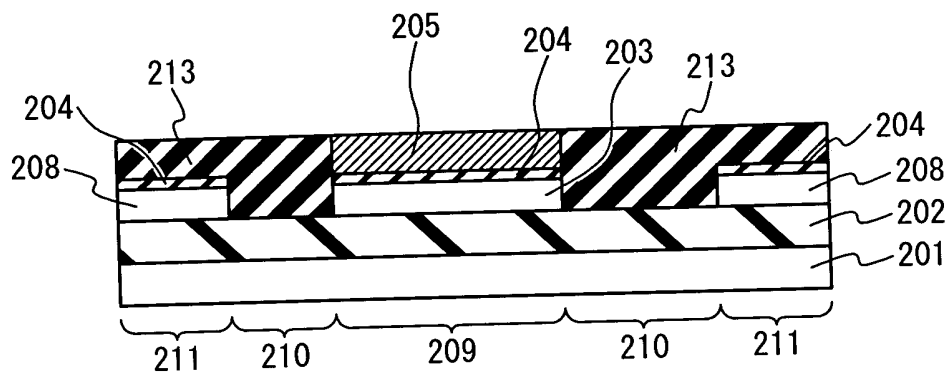


Fig. 14C

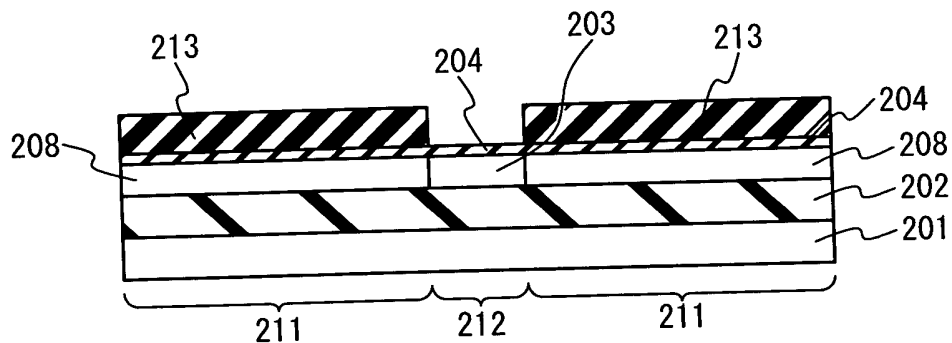


Fig. 15

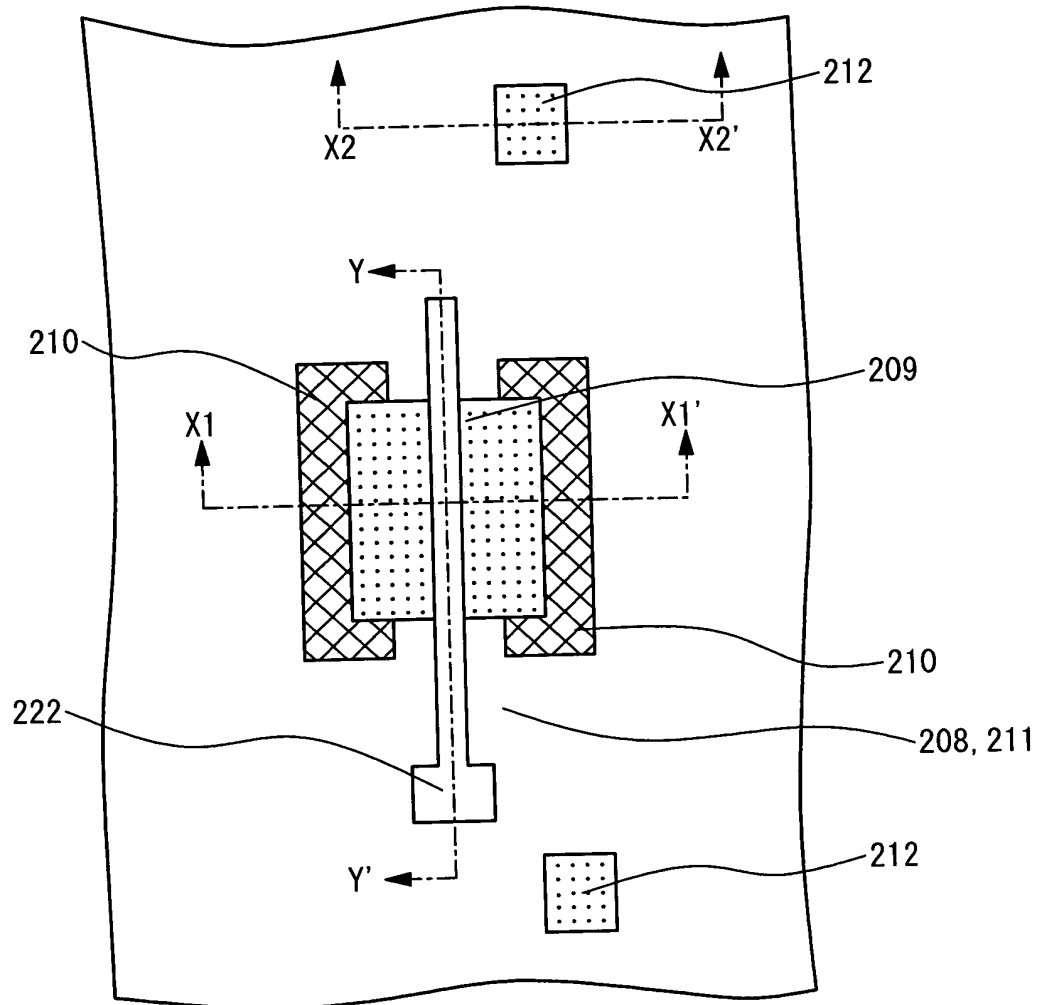


Fig. 16A

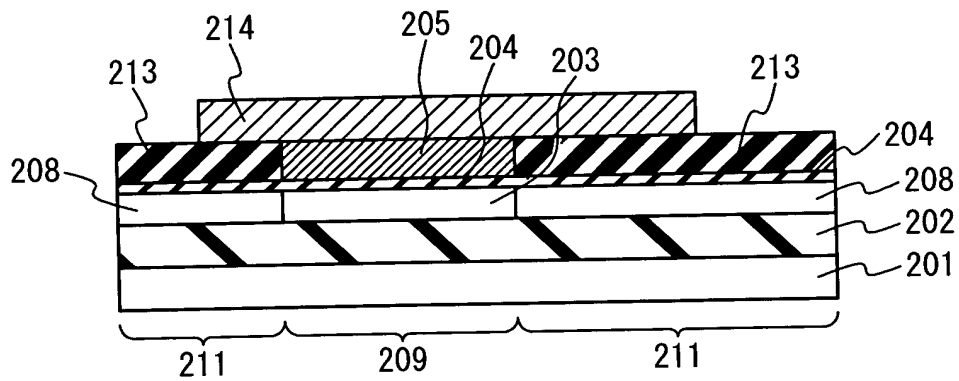


Fig. 16B

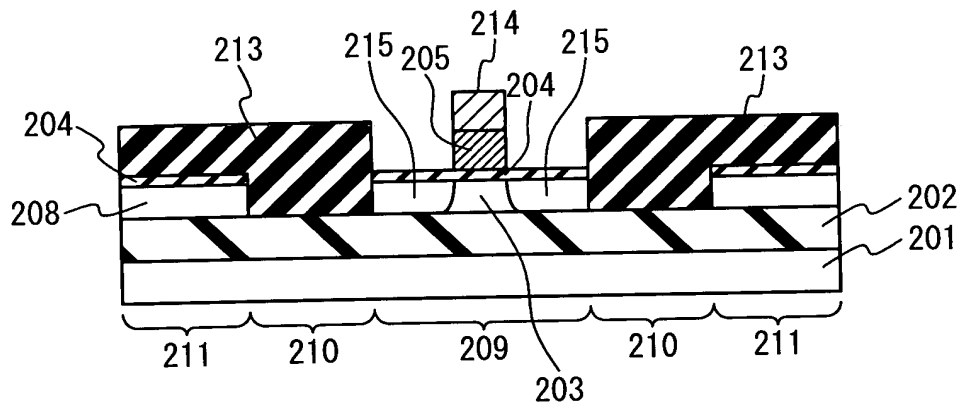


Fig. 16C

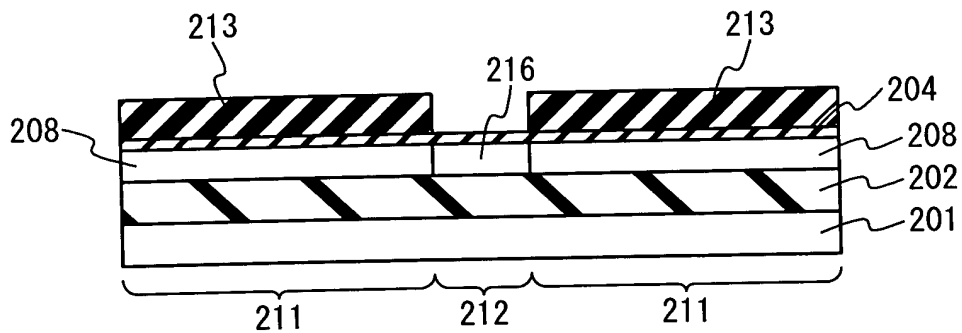


Fig. 17A

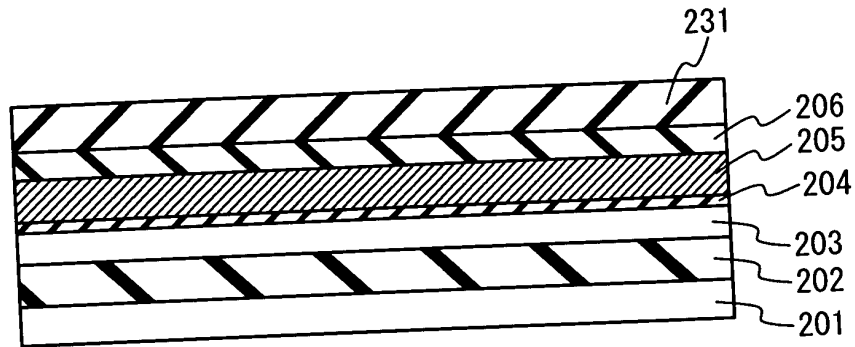


Fig. 17B

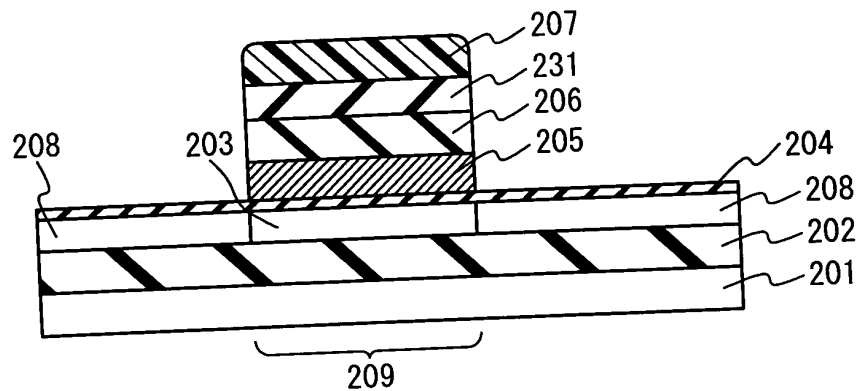


Fig. 18A

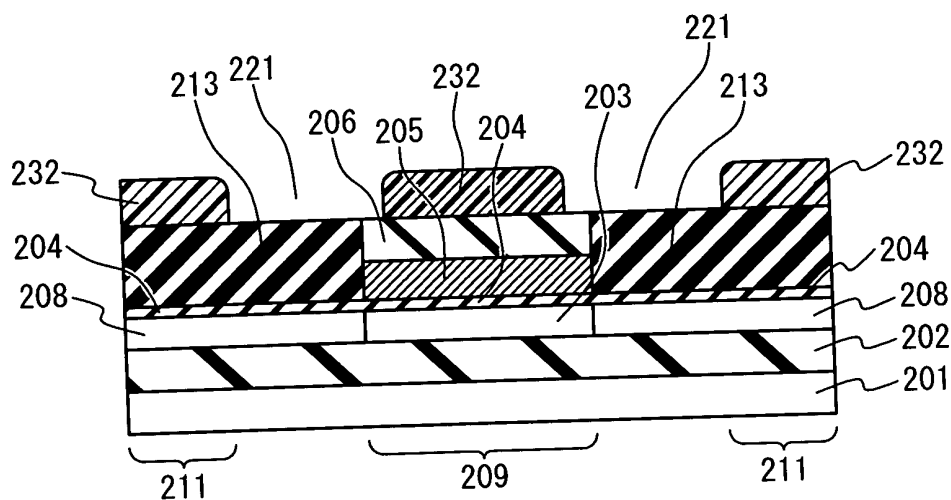


Fig. 18B

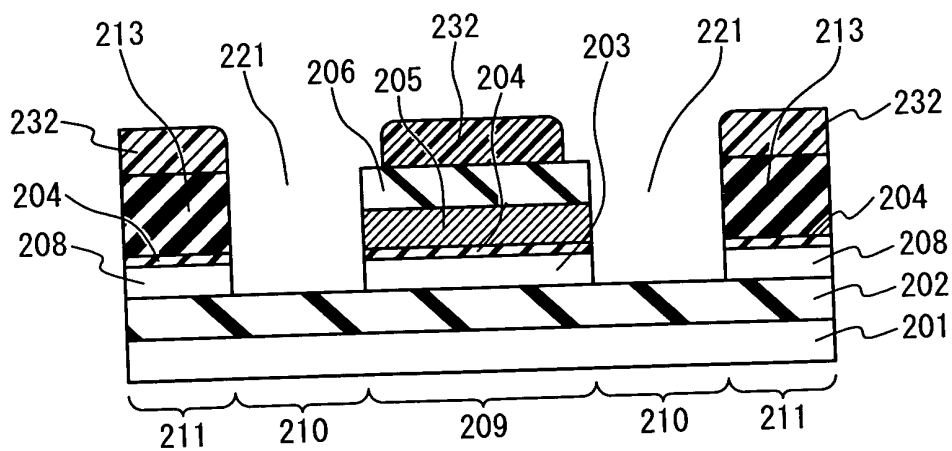


Fig. 19A

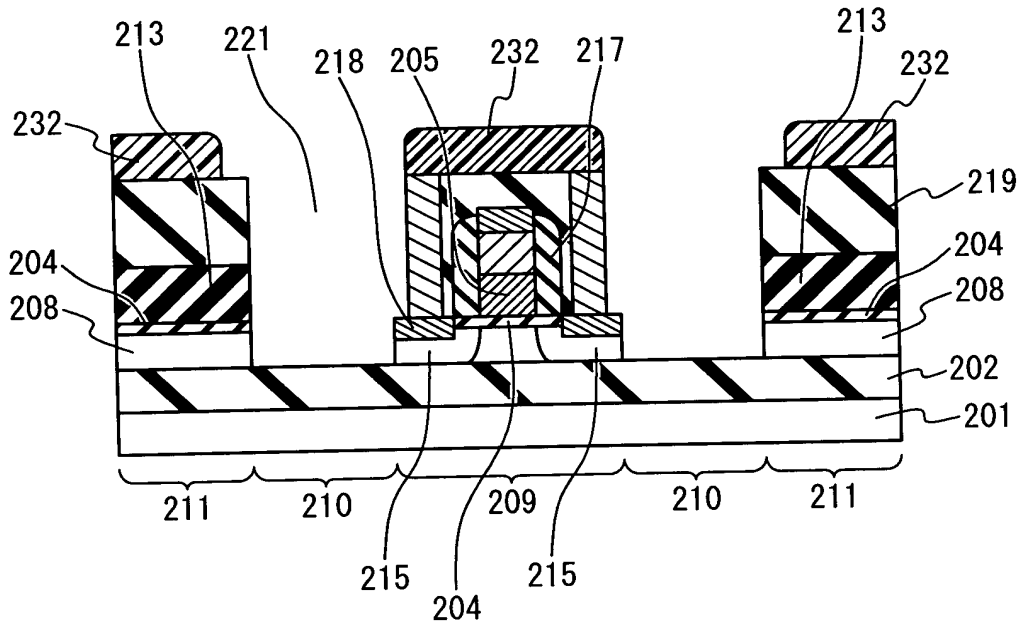
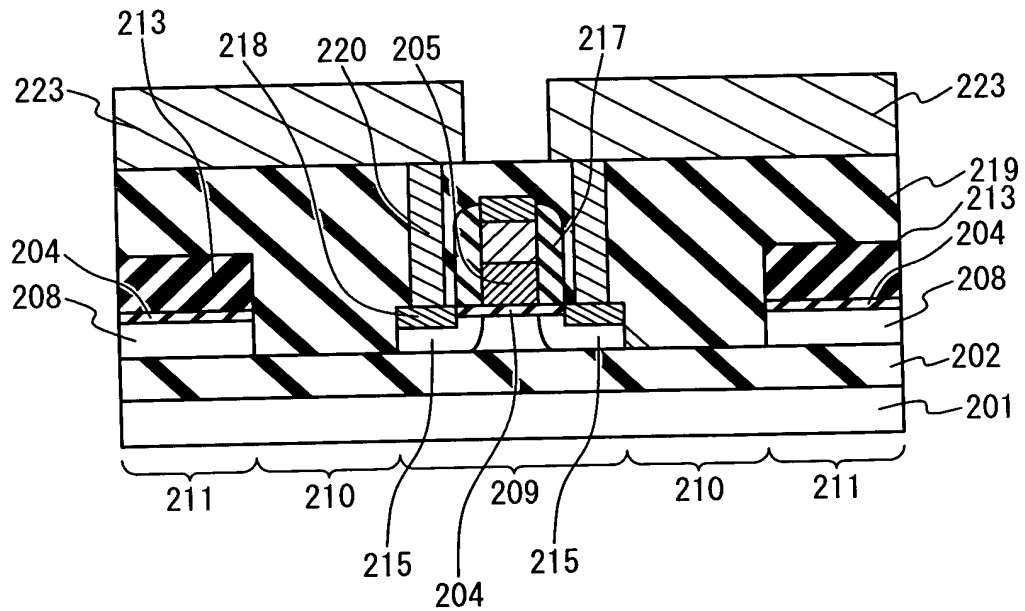


Fig. 19B



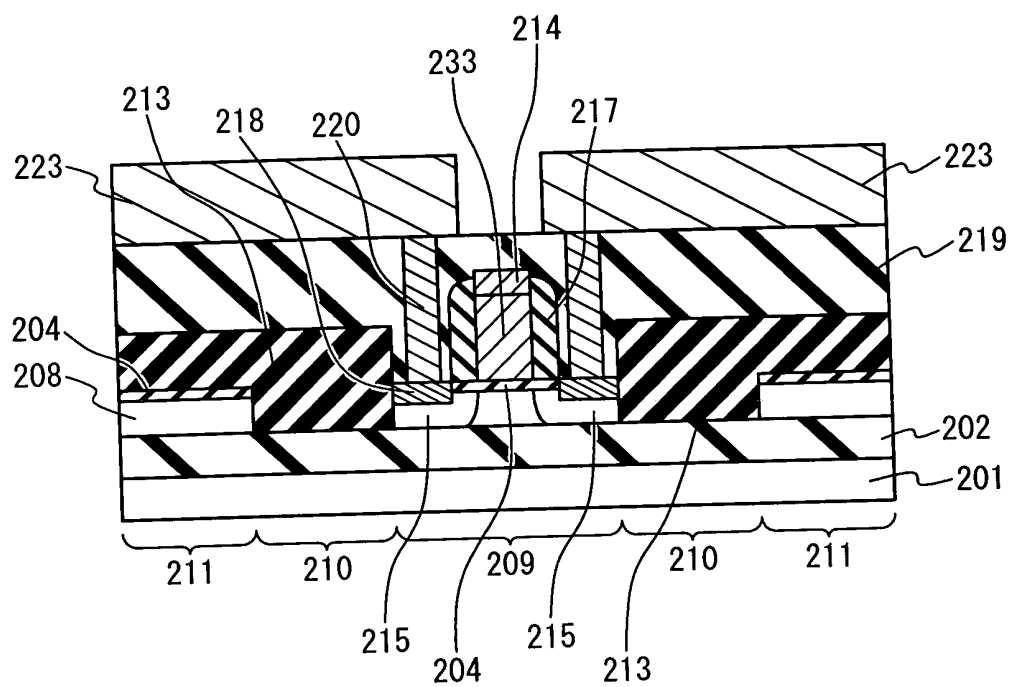
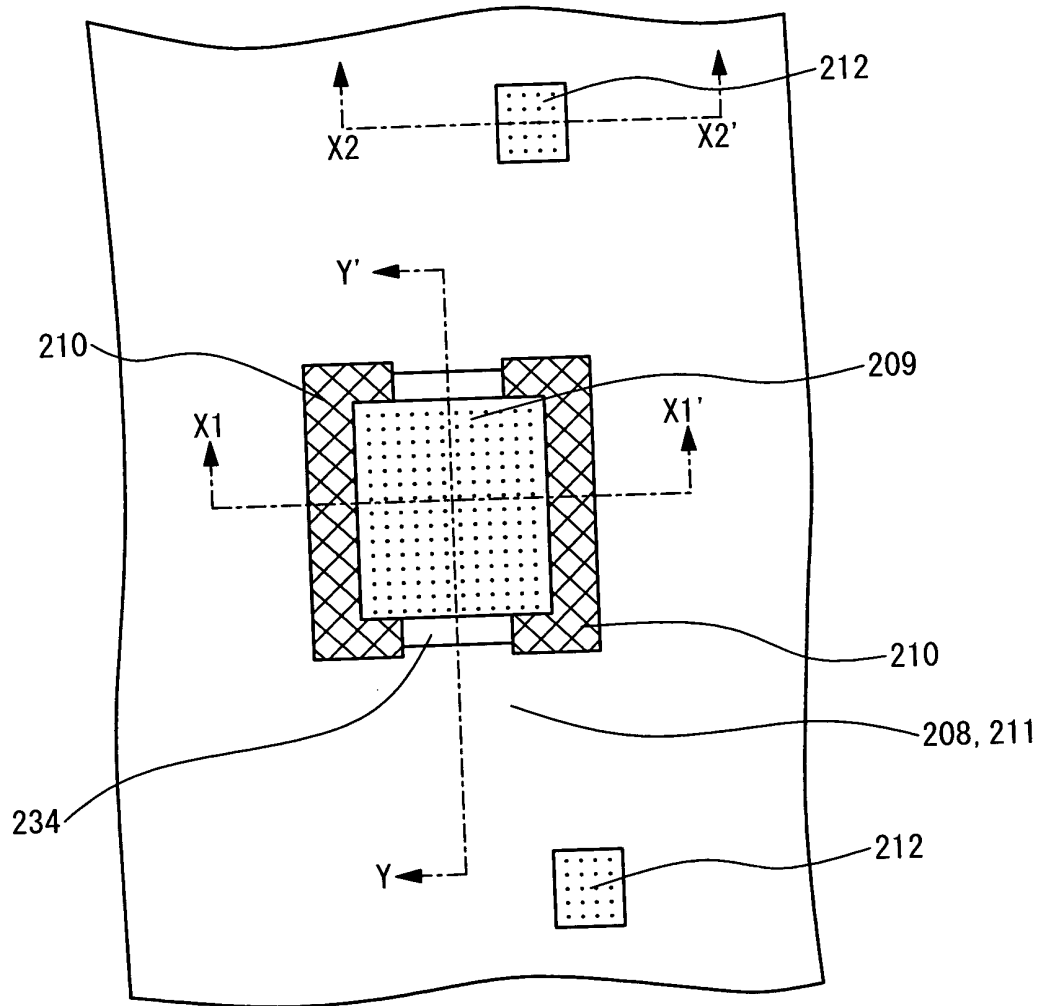
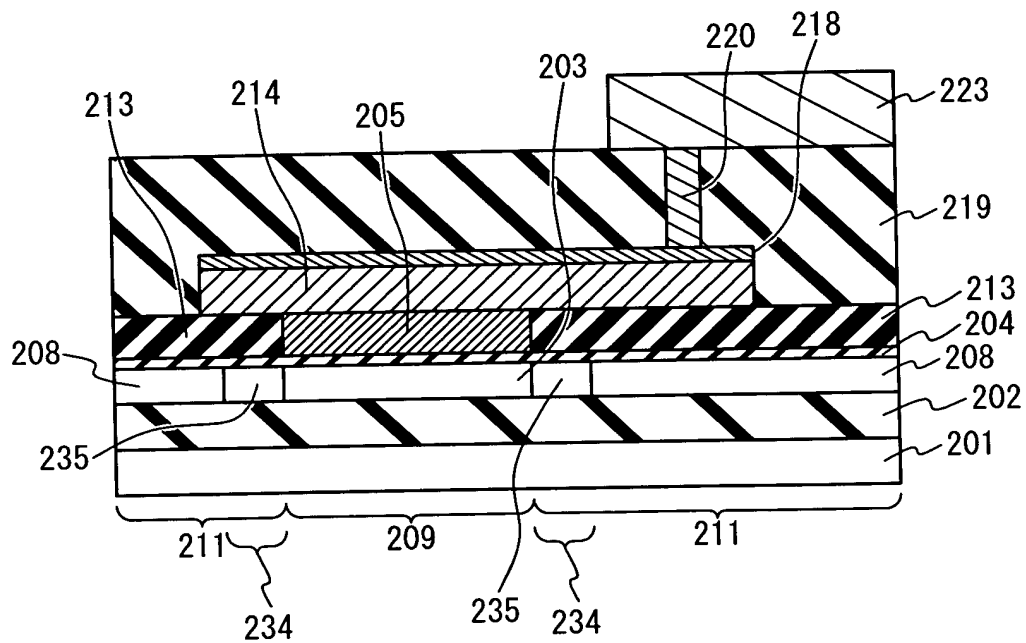
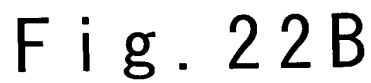


Fig. 21





A cross-sectional view of a semiconductor device. The device consists of a substrate with multiple layers. From bottom to top, the layers are labeled 201, 202, 203, 204, 205, 206, and 208. A central region 209 is defined by a bracket below the substrate, flanked by two regions labeled 234. The top surface of the device is labeled 236.

A cross-sectional view of a semiconductor device. The device consists of a substrate 201 with multiple layers 202 and 204. A central structure 203 is formed on the substrate, containing a core 205 and a surrounding layer 206. The central structure is flanked by regions 208. The entire device is covered by a top layer 209. Brackets indicate regions 234 and 235. Labels 236 point to specific features on the top surface of the central structure.

Fig. 24A

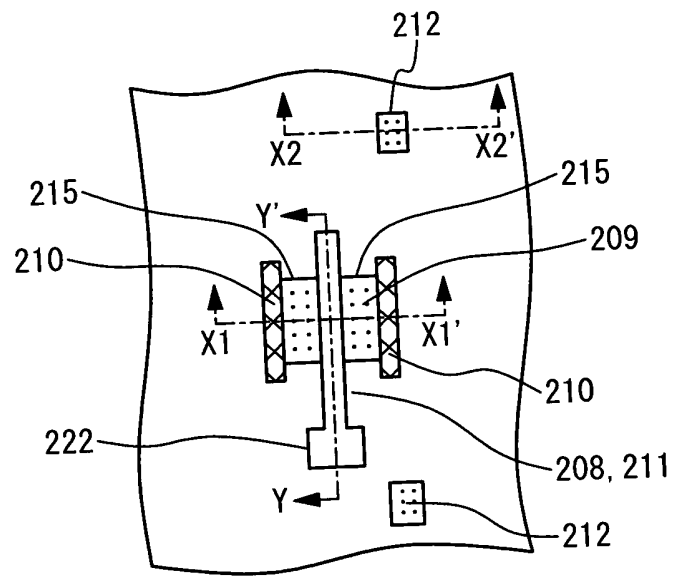


Fig. 24B

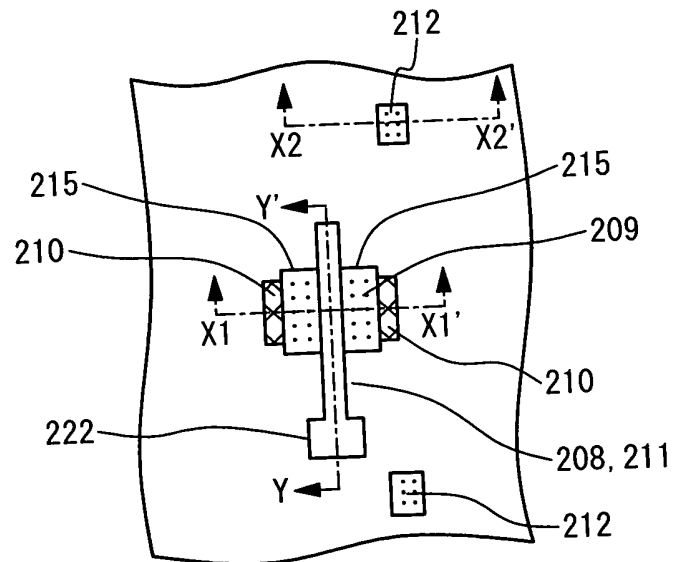


Fig. 25A

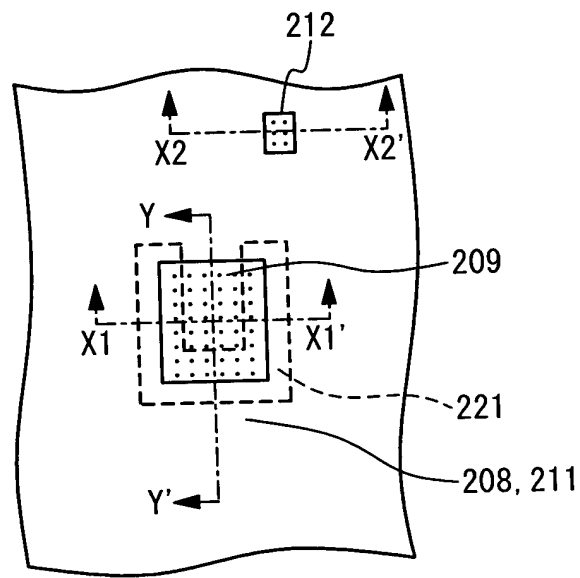


Fig. 25B

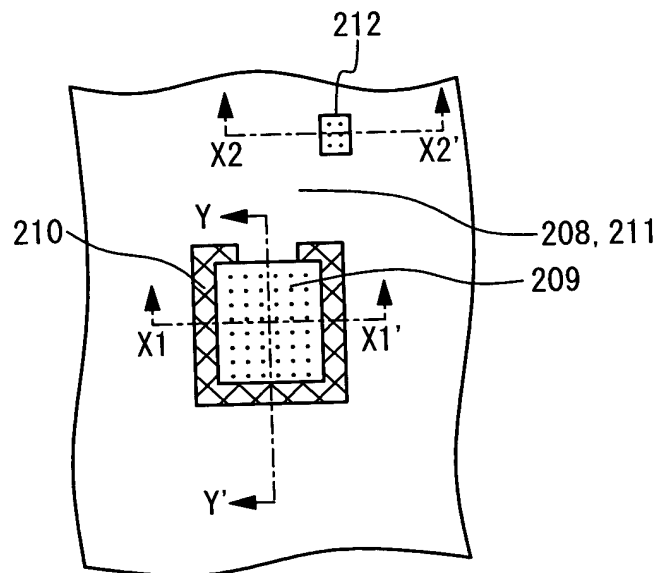


Fig. 26A

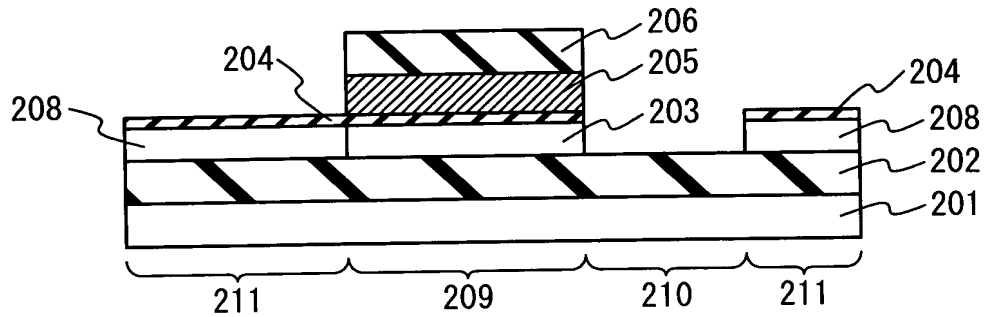


Fig. 26B

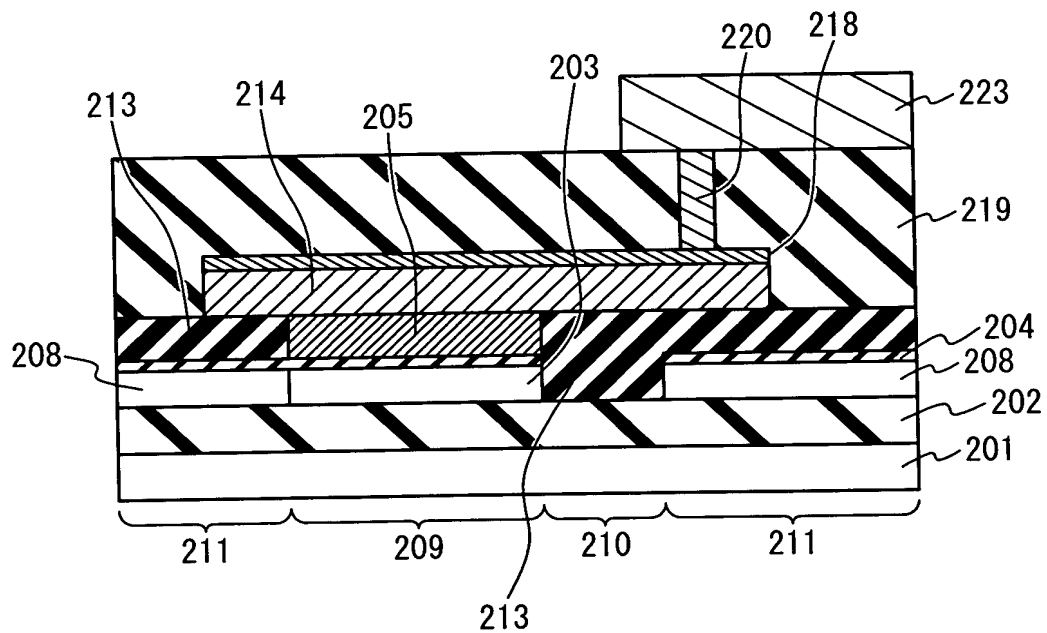


Fig. 27A

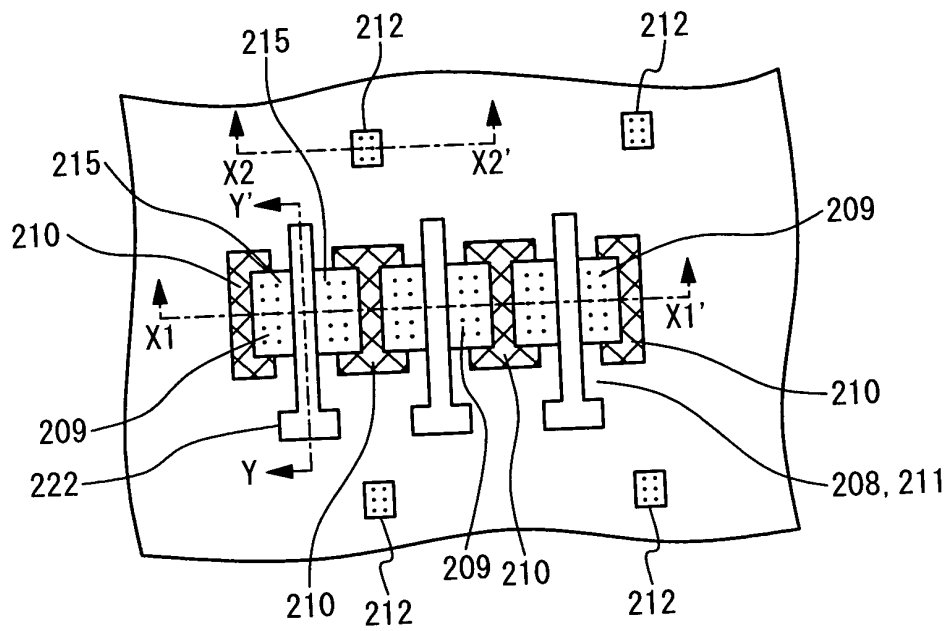


Fig. 27B

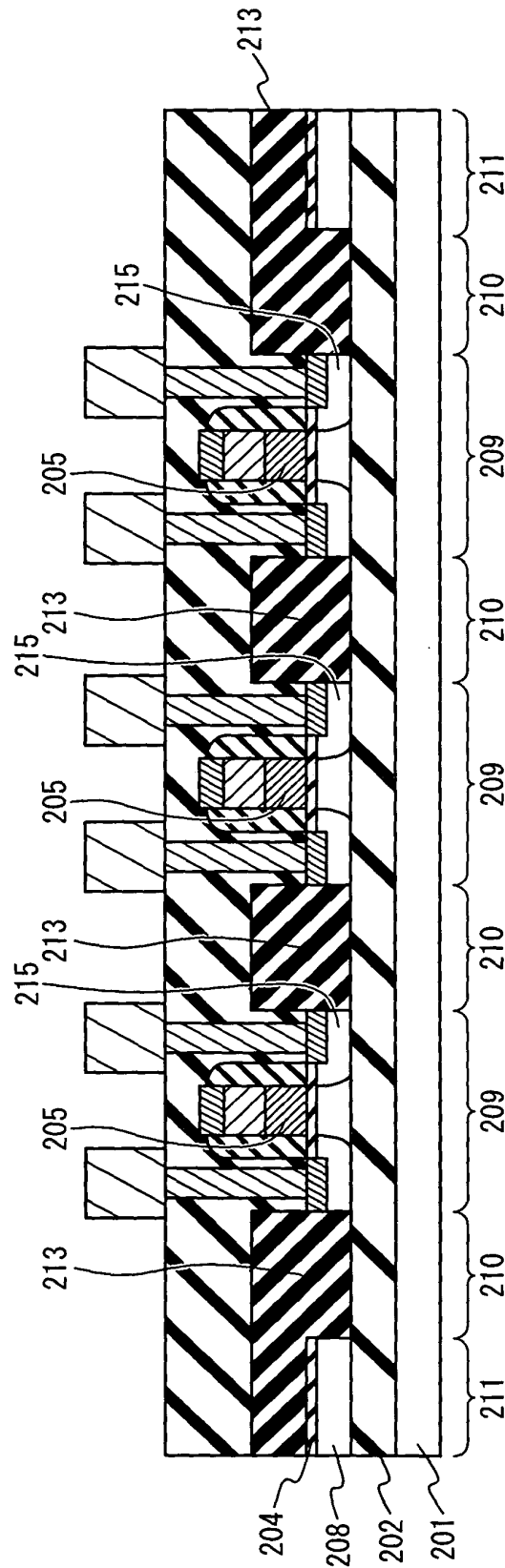


Fig. 28A

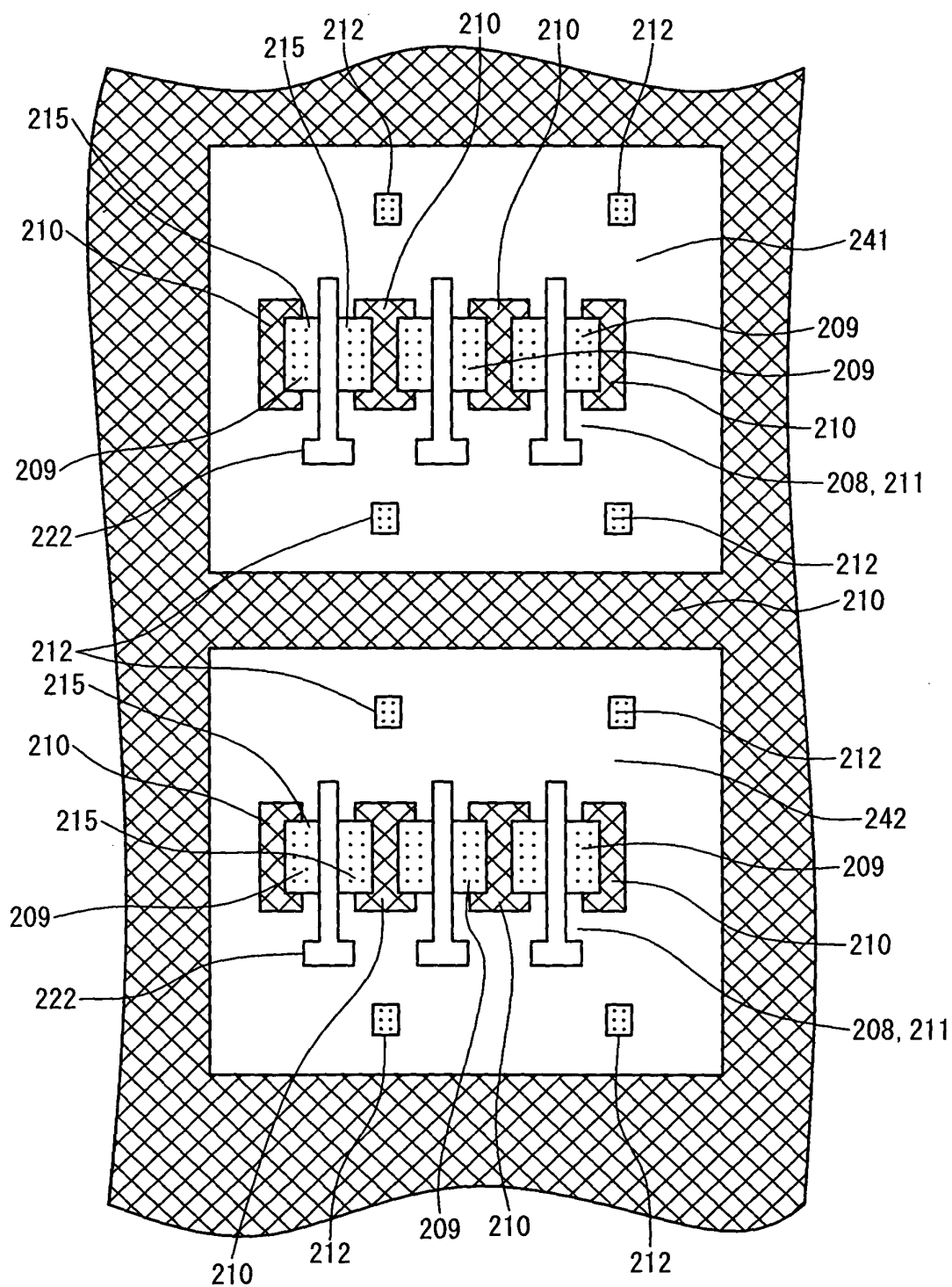


Fig. 28B

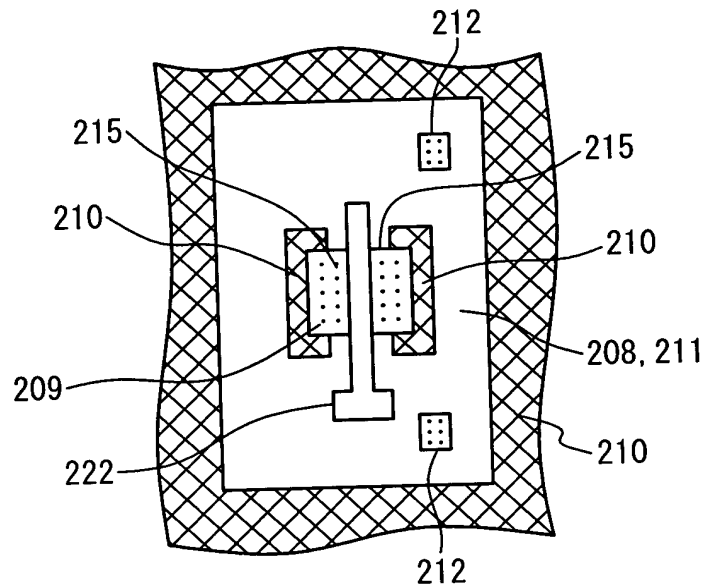


Fig. 28C

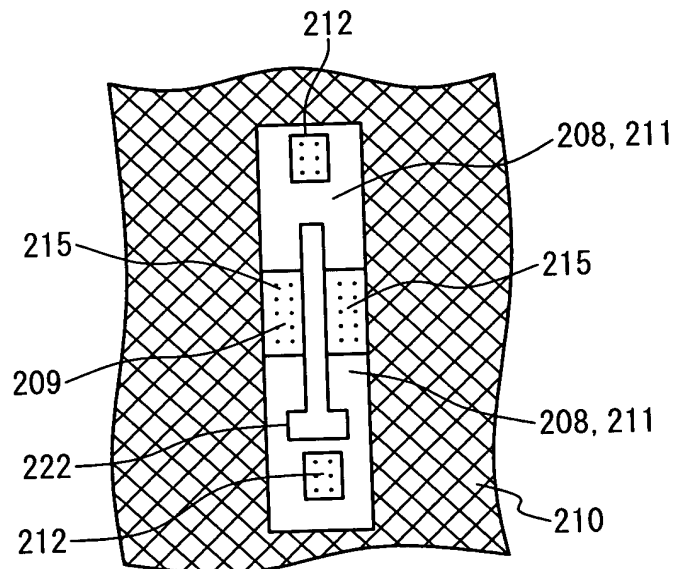


Fig. 28D

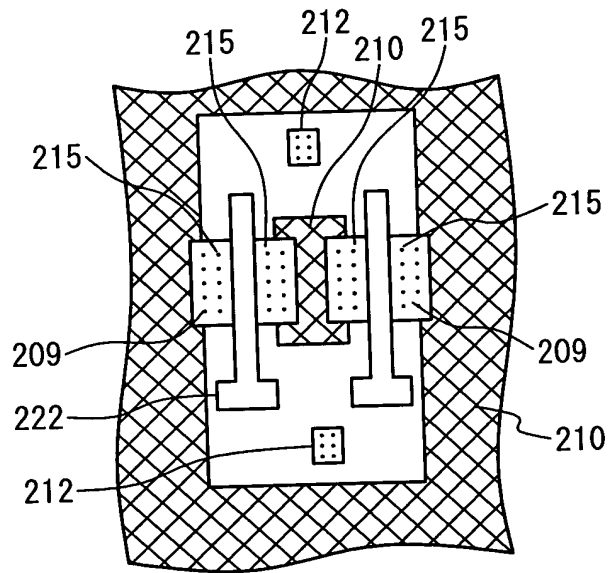


Fig. 28E

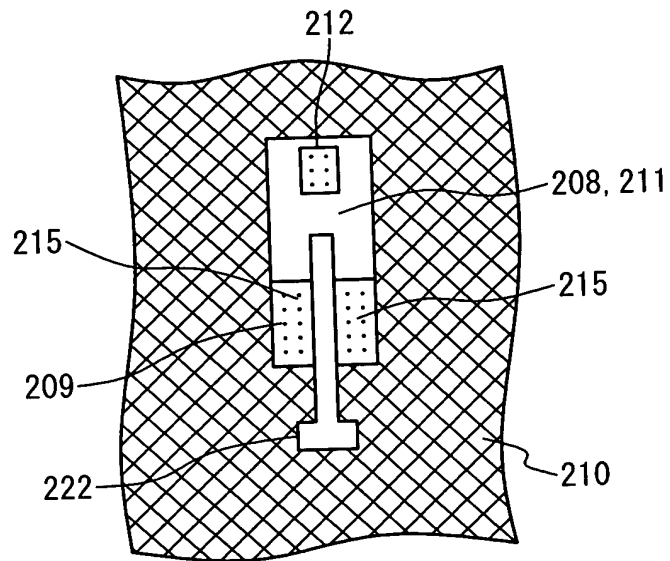


Fig. 28F

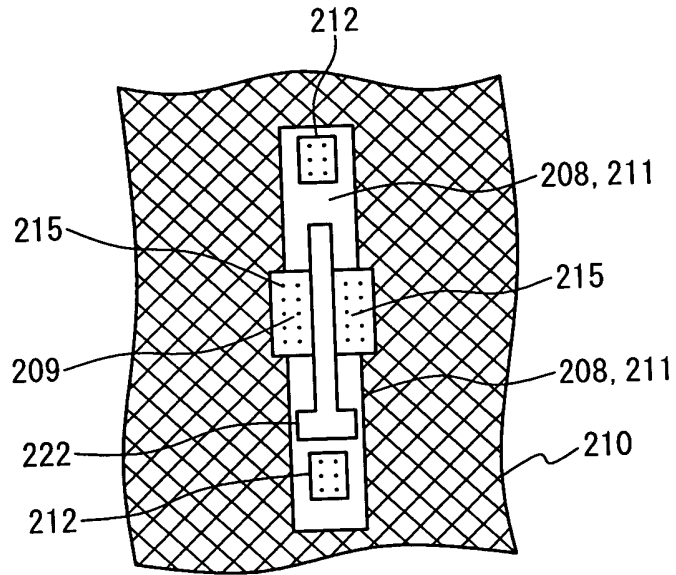


Fig. 28G

